Remarks

By this response the specification has been amended to include the status of the parent case of which this application is a divisional.

Claim Rejection 35 U.S.C. § 102

The Examiner rejected claims 8 - 10 under 35 U.S.C. § 102(b) as being anticipated by Nelson et al, Pat. No. 6,449,200 ('200 patent).

The Examiner indicated that the '200 patent discloses an active restore circuit for write margin testing of an SRAM having a bitline restore driver comprising: a NAND gate (fig. 7, 86 and 87) connected to the bitline restore driver (fig 7, 72 and 73) having three terminals; a write margin test signal is applied to the first NAND gate terminal to activate the margin test (fig. 7, TEST); a sub array clock signal (fig 7, 81 Clock) is applied to the second terminal of the NAND gate which generates a restore signal to the bitline restore driver to block the bitline restore devices from turning off during the SRAM write cycle (col 7, line 7-43).

With regard to claim 9, '200 patent discloses two transistors in the bitline restore driver to assist the bitline driver to block the bitline restore devices from turning off (Fig. 7, 77).

With regard to claim 10, '200 patent discloses wherein cells are identified if they fail the write test margin test (col. 3, line 44-55) (col. 8, line 28-43).

The Inventor of the present invention is quite familiar with the '200 patent because all the inventors of the '200 patent are colleagues employed by International Business Machines Corporation which is the common assignee and therefore the person which obtained the '200 patent and person involved in the subject patent application. The using the '200 patent and the appropriateness of the '200 patent as a reference against this application will be discussed later herein. The Inventor understands that the '200 patent is directed to a testing technique for SRAM but does not believe it anticipates claims 8-11. He points out, for example, in Fig. 7 elements 86 and 87 are part of the address generators (see col. 6, line 49) and therefore not part of the bitline restore driver as indicated by the Examiner as the basis for rejection under 35 U.S.C. § 102(b). The Examiner also indicated that the use of circuit block 70 (col. 7,line 7-43) is used to generate a restore signal to the bitline restore driver to block the bitline restore devices from turning off during the SRAM write cycle. However, the Inventor states that in actuality circuit block 70 in the '200 patent is the address generator and not the circuit being used to prevent the bitline restore from turning off.

With regard to Claim 9, the device 77 in Fig. 7 in the '200 patent that the Examiner indicated was used to block the bitline restore devices from turning off during the SRAM write cycle. However, the inventor points out that device 77 actually forms the write bit switches and are not associated with the bitline restore. If the Examiner wishes, the Inventor is willing to enter these observations by way of an Affidavit.

Based on the foregoing, it is respectfully submitted that Claims 8 and 9 are allowable under 35 U.S.C. § 102(b) as well as all other claims that depend on claims 8 and 9, namely, claims 10 and 11..

Claim Rejection 35 U.S.C. § 103

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Nelson, et al, Pat No 6,449,200 ('200 patent) in view of Lee, Pat. No. 5,748,543.

The Examiner indicated that in claim 11, the '200 patent is applied as in the prior 35 U.S.C. § 102(b) rejection, and disclosed all claimed subject matter except wherein the identified failed cells are replaced with redundant memory elements. However, Lee discloses that it is well known in the semiconductor art, if a failed cell is detected in a regular memory cell array during testing, the failed memory cell is replaced by a spare memory cell in the spare memory cell (col. 1, line 21-26). Therefore it would have been

obvious for one having an ordinary skill in the art at the time the invention was made to incorporate concept of replacing the defective memory cell with a redundant memory cell in Lee's device into the '200 patent to reduce the manufacturing cost and increase the manufacturing yields of chips.

The applicant respectfully wishes to point out that not all claimed subject matter is disclosed in the '200 patent as discussed above. Additionally, the applicant respectfully submits that because claims 8-10 are allowable that claim 11 which depends on claims 8-10 should also be allowable.

Applicant also respectfully submits that the '200 patent issued to Nelson, et al. should not be applied because the '200 patent and the invention claimed herein are owned by the same person (namely, International Business Machines, Inc.) under 35 U.S.C. § 103(c). Please note that the subject application was based upon a parent case filed on 7/26/2002 that is prior to the issuance of Nelson, et al. (September 10, 2002). As such, the '200 patent should not be individually or combined with Lee, et al. to preclude patentability of Applicant's claims.

Based on the foregoing, it is submitted that Claim 11 should be allowable under 35 U.S.C. § 103(a).

Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Geordie Braceras

By: Robert A. Walsh

Robert A. Walsh
Registration No. 26,516
Telephone No.: (802) 769-9521
Fax No.: (802)769-8938

International Business Machines Corporation
Intellectual Property Law - Mail 972E
1000 River Road
Essex Junction, VT 05452